Comparison of Ultra-Low-Power and static CMOS full adders in 0.15 µm FD SOI CMOS

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***Abstract*—Ultra-low-power and static CMOS full adders are implemented in a 0.15 µm FD SOI CMOS technology with 1.5V supply. The power consumption of ultra-low-power full adder is shown to be half that of static CMOS. These results are confirmed by both measurements and SPICE simulations in different corners of operation.**

I. Introduction

The full adder (FA) is a very important basic building block in many types of applications, from high performance to ultra-low power (ULP) such as e.g. RFID. Therefore, reducing its power consumption is a major objective as it directly affects the total power of the system. High-security applications may also benefit from low-power logic operation, to increase cryptographic functions at same cost and resistance against power measurement attacks [1].

Two FA types are studied, the static CMOS [2] as a reference (Fig. 1) and our proposed Ultra-Low-Power full adder (ULP FA, Fig. 2) [3]. The former is well known for its robustness and scalability at low supply voltages. However, its power consumption and transistor count (28) are relatively high for low-power arithmetic circuits. Simulations of ULP FA have shown promising reduction of power consumption [3]. Its carry part uses branch-based logic and its sum part uses low-power XOR gates from [4]. As the XOR gate suffers from a weak "0" logic output for (0,0) input configuration, the use of novel ULP diode (ULPD) architecture [5] is suggested to restore the correct output level with strongly reduced leakage current, thanks to its negative-differential-resistance I/V characteristics. The ULPD features an n-MOSFET on top of a p-MOSFET with common sources and respective gates connected to the drain of the other MOSFET. The ULP FA thus counts 24 transistors.

II. Measurement results and discussion

Both FAs are fabricated in 0.15µm fully-depleted (FD) SOI CMOS technology. Fig. 3 shows a block diagram of the measurement test bench, where the C input of the FA under test is driven by two inverters having an alternating "10" input test pattern with 50 % duty cycle at frequencies from a few Hz to 100 MHz, while the A and B inputs are at supply voltage V_{DD} and ground, respectively. The sum and carry outputs are loaded by dummy 1-bit FAs of the same kind.

Fig. 4 and 5 show our measurement and simulation results, with typical and worst-case corners included, of the static CMOS and the ULP FAs respectively, for nominal V_{DD} = 1.5V. Their power consumption ratios are shown in Fig. 6. Theoretical results for 0.13µm CMOS indicated in [3] a power consumption of 0.5 µW at 100 MHz for the ULP FA, lower by a factor of 2.8 than that of the static CMOS, but these results were obtained at schematic level (prior to layout) i.e. with no load and rough estimation of routing capacitances. Simulations of an 8-bit RCA adder taking loading and routing into consideration still indicated a reduced power by a factor of 2 for the ULP adder [3]. The average measured power P_{avg} is slightly higher than the simulation results of [3] due to the load and routing capacitances, but the power consumption advantage of the ULP FA confirms the expected factor of 2 above 100 kHz (Fig. 6).

The standard deviation of the power consumption σ(P) was extracted on ten dies. The insets in Fig. 4 and 5 show the relative value $\sigma(P)/P_{avg}$ to be similar for the two FAs. It is below 5 % for frequencies above 100 kHz, in which region dynamic power dominates. However, below 10 kHz, static power dominates and $\sigma(P)/P_{avg}$ rises to 40 %. To the first order, a lower bound on $\sigma(P)/P_{avg}$ is given by $\sigma(I_d)/I_d$ provided that frequency, V_{DD} and capacitances do not vary significantly. From matching theory, $\sigma(I_d)/I_d = (g_m/I_d).\sigma(V_{th}) + \sigma(\beta)/\beta$ where V_{th} is the threshold voltage and β the usual "$\mu.C_{ox}.W/L$" factor. Our power measurements follow this trend with $\sigma(V_{th}) \approx$ 10mV and $\sigma(\beta)/\beta \approx$ 2-3%, considering respectively for static (I_{off}) to dynamic (short-circuit current) power that g_m/I_d physically varies from about 30 V^{-1} in subthreshold to 2-3 V^{-1} in strong inversion. A small power variation is an asset to guarantee consistency in performance for most applications but from physics, the static power cannot be better controlled, without increasing device sizes to lower V_{th} and β variability, which could be acceptable for low-frequency operation such as in RFID. However, the variability of the power consumption pattern between different dies could be of interest for security applications to prevent code or data deciphering by power measurements.

Fig. 4 and 5 also show power consumption simulations for the typical (TT), slow (SS) and fast (FF) corners. Experimental results appear closer to FF. The static power consumption ratio of static CMOS to ULP FAs ($Power_{SC}/Power_{ULP}$) is obviously

exacerbated by variability (Fig. 6), but due to model inaccuracy the simulation results show a ratio less than two for all corners.

III. Conclusion

Measurements of ULP full adder in 0.15µm FD SOI CMOS demonstrate significant power reduction with respect to conventional static CMOS design, by a factor of about 2 in a wide range of operating frequency. Both adders show similar relative standard deviation. The measurement results are in good agreement with simulations.

Acknowledgement

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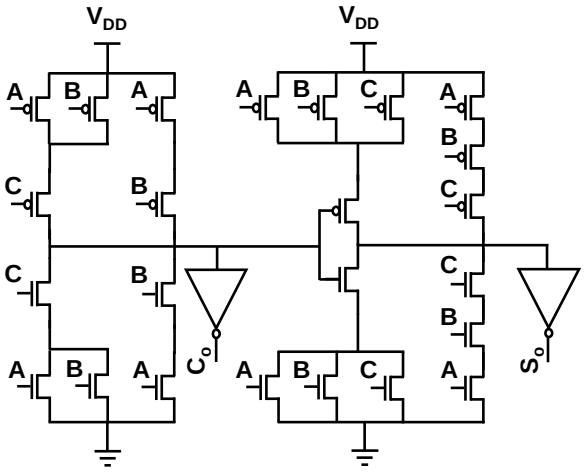

Fig. 1. Conventional static CMOS 1 bit full adder schematic.

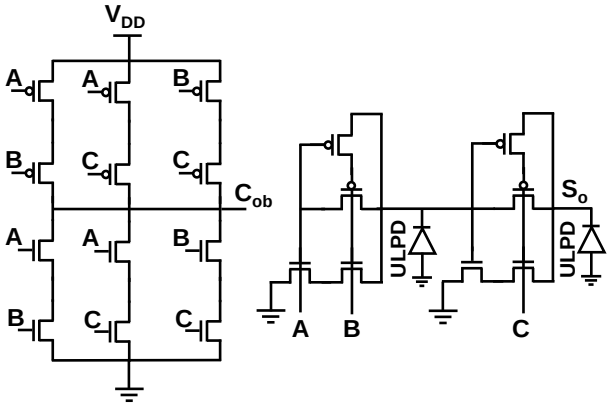

Fig. 2. Ultra low-power (ULP) 1 bit full adder schematic [3].

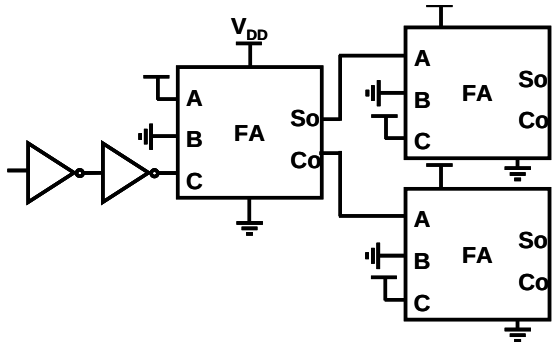

Fig. 3. Block diagram of measurement test bench arrangement.

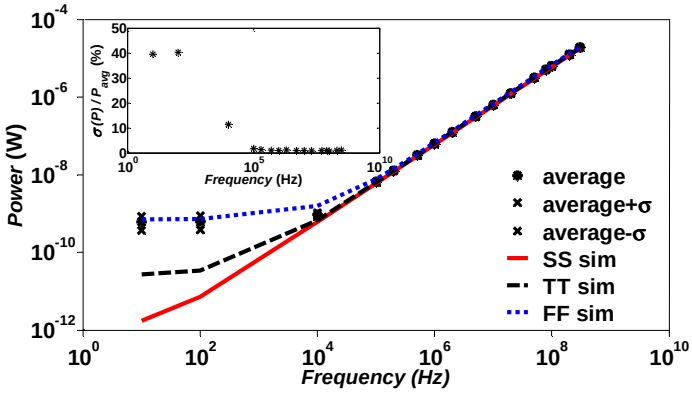

Fig. 4. Measured and simulated power consumption of static CMOS 1 bit FA (TT, FF and SS refer to process corners on n- / p-MOSFETs). The inset shows $\sigma(P)/P_{avg}$ variation with frequency.

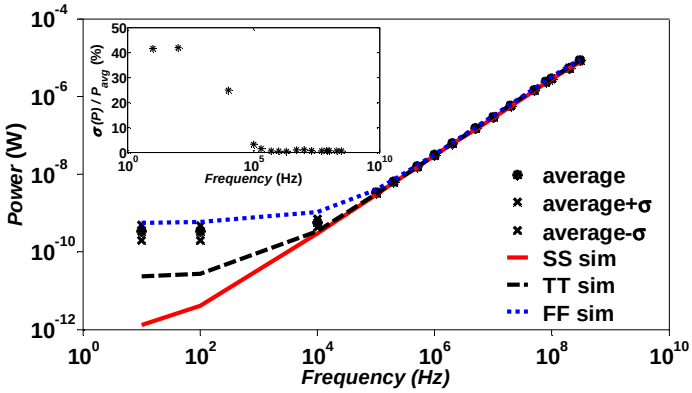

Fig. 5. Measured and simulated power consumption of ULP 1 bit FA. The inset shows $\sigma(P)/P_{avg}$ variation with frequency.

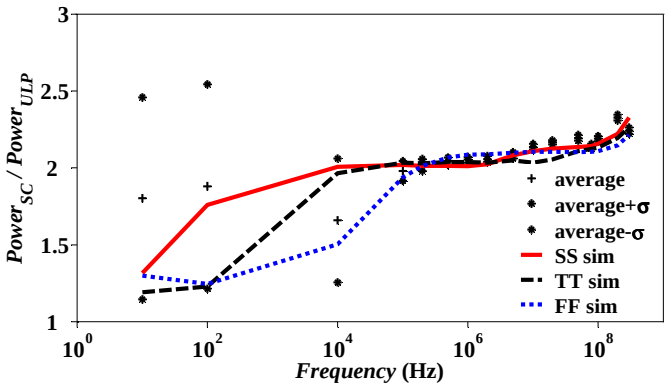

Fig. 6. Measured and simulated power consumption ratio of static CMOS to ULP 1 bit FAs